EXAMPLE 3

[0079] Example 3 relates to the spin tunnel transistor in the second embodiment.

[0080] Using the same process as that in the example 1, a spin tunnel transistor was formed on a Si substrate 1 through a $CoSi_2$ layer 3 of about 1 nm thickness, which included a Cu layer 15 (about 5 nm thickness), a $Ni_{81}Fe_{19}$ layer 9 (about 4 nm thickness), an Al_2O_3 layer 11, and a Fe layer 17 (about 10 nm thickness). On the Fe layer 17 was formed an Au electrode of about 100 nm thickness.

[0081] In the transistor, the current transmittance and MR ratio at an emitter voltage of about 1.5 V were about 4.1×10^{-2} and about 101% respectively, and the current transmittance and MR ratio at an emitter voltage of about 2 V were about 5.5×10^{-2} and about 96.6% respectively.

COMPARATIVE EXAMPLE 3

[0082] A spin tunnel transistor including an Au layer of about 1 nm thickness instead of the $CoSi_2$ layer of about 1 nm thickness in the example 3 was prepared using the same process as that in the example 2. In the transistor, the current transmittance and MR ratio at an emitter voltage of about 1.5 V were about 3.9×10^{-3} and about 93% respectively. The transistor exhibited a current transmittance one or more orders of magnitude lower than that the transistor of the example 2 did.

EXAMPLE 4

[0083] Example 4 relates to the spin tunnel transistor in the second embodiment.

[0084] Using the same process as that in the example 2, a spin tunnel transistor was formed on a Si substrate 1 through a Pd layer 3 of about 1 nm thickness, which had a Cu layer 15 (about 5 nm thickness) and a $Ni_{81}Fe_{19}$ layer 9 (about 4 nm thickness) of the base, an Al_2O_3 barrier layer 11, and a $Co_{84}Fe_{16}$ layer 17 (about 10 nm thickness). On the $Co_{84}Fe_{16}$ layer 17 was formed an Au electrode of about 100 nm thickness.

[0085] In the transistor, the current transmittance and MR ratio at an emitter voltage of about 1.5 V were about 3.2×10^{-2} and about 62% respectively, and the current transmittance and MR ratio at an emitter voltage of about 2 V were about 4.4×10^{-2} and about 60.4% respectively.

[0086] While the embodiments of the invention have been described above, the invention is not so limited and various changes may be made within the scope of the subject matter of the invention as defined in the claims.

[0087] Also, in practicing the invention, various modifications may be made without departing from the subject matter of the invention.

[0088] Further, variations are possible by appropriate combinations of constituent elements disclosed in the above embodiments. For example, some of the all constituent elements shown in the embodiments maybe deleted. Also, the constituent elements may be appropriately combined across the different embodiments.

What is claimed is:

1. A spin tunnel transistor comprising:

a collector;

an emitter;

a base formed between the collector and the emitter, the base comprising a first ferromagnetic metal layer variable in its magnetization under an external magnetic field;

a barrier layer formed between the base and one of the collector and the emitter, the other of the collector and the emitter comprising a semiconductor crystal layer; and

a palladium layer between the semiconductor crystal layer and the base.

2. The spin tunnel transistor of claim 1, wherein the base further comprises:

a non-magnetic metal layer on the first ferromagnetic metal layer; and

a second ferromagnetic metal layer stacked via the first non-magnetic metal on the first ferromagnetic metal layer, the second ferromagnetic metal layer having a magnetization substantially fixed under the external magnetic field.

3. The spin tunnel transistor of claim 1, wherein the barrier layer is formed between the base and the collector, the collector comprises a second ferromagnetic metal layer, and the second ferromagnetic metal layer has a magnetization substantially fixed under the external magnetic field.

4. The spin tunnel transistor of claim 1, wherein the barrier layer is formed between the base and the emitter, the emitter comprises a second ferromagnetic metal layer, and the second ferromagnetic metal layer has a magnetization substantially fixed under the external magnetic field.

5. A magnetic random access memory, comprising the spin tunnel transistor of claim 1.

6. A magnetic reproducing head, comprising the spin tunnel transistor of claim 1.

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